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Xie, H.A.; Forward, K.E.; Adams, K.M.; Leask, D.;
Field-Programmable Gate Arrays, 1995. FPGA '95. Proceedings of the Third Internatio
Symposium on
1995 Page(s):160 - 167
AbstractPlus | Full Text: PDF(128 KB) IEEE CNF

2. **An SBus Multi Tracer and its applications**
Xie, H.A.; Forward, K.; Adams, K.M.; Kumar, S.;
Test Symposium, 1995., Proceedings of the Fourth Asian
23-24 Nov. 1995 Page(s):9 - 14
AbstractPlus | Full Text: PDF(460 KB) IEEE CNF

3. **Development of board level simulation models of complex standard components**
Pottinger, D.H.J.; Williams, G.R., III; Kelly, J.S.; Tamboli, S.;
Circuits and Systems, 1996., IEEE 39th Midwest symposium on
Volume 1, 18-21 Aug. 1996 Page(s):415 - 418 vol.1
AbstractPlus | Full Text: PDF(420 KB) IEEE CNF

4. **AKKA: a tool-kit for cosynthesis and prototyping**
Tammemae, K.; O'Nils, M.; Jantsch, A.; Hemani, A.;
Hardware-Software Cosynthesis for Reconfigurable Systems (Digest No: 1996/036), IE
22 Feb. 1996 Page(s):8/1 - 8/8
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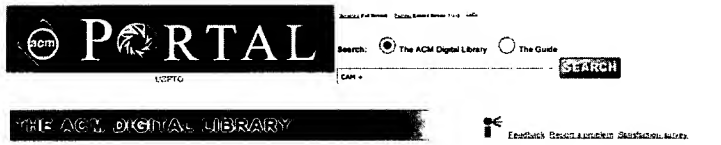

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1 A Configurable Logic Architecture for Dynamic Hardware/Software Partitioning
Roman Lysecky, Frank Vahid
February 2004 **Proceedings of the conference on Design, automation and test in Europe - Volume 1**
Full text available: pdf(111.60 KB) Additional information: full citation, abstract, citings, index terms

In previous work, we showed the benefits and feasibility of having a processor dynamically partition its executing software such that critical software kernels are transparently partitioned to execute as a hardware coprocessor on configurable logic -- an approach we call warp processing. The configurable logic place and route step is the most computationally intensive part of such hardware/software partitioning, normally running for many minutes or hours on powerful desktop processors. In contra ...

Keywords: Hardware/software partitioning, FPGA fabric, configurable logic, synthesis, place and route, platforms, system-on-a-chip, dynamic optimization, codesign, self-improving chips, just-in-timecompilation, warp processors, reconfigurable computing

2 A hardware implementation of gridless routing based on content addressable memory
Masao Sato, Kazuto Kubota, Tatsuo Ohtsuki
January 1991 **Proceedings of the 27th ACM/IEEE conference on Design automation**
Full text available: pdf(474.47 KB) Additional information: full citation, abstract, references, citings, index terms

A new gridless router accelerated by Content Addressable Memory (CAM) is presented. A gridless version of the line-expansion algorithm is implemented, which always finds a path if one exists. The router runs in linear time by means of the CAM-based accelerator. Experimental results show that the more obstacles there are in the routing region, the more effective the CAM-based approach is.

3 A high performance routing engine
T. D. Spiers, D. A. Edwards
October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation**
Full text available: pdf(514.84 KB) Additional information: full citation, abstract, references, citings, index terms

A hardware architecture for implementing Lee based routing algorithms is described. The design features hardware implementations of the main data structures and parallelism among a number of specialised processing elements. An engine based on this architecture has been constructed which executes a sophisticated cost-based algorithm 40 times faster than a VAX 11/780.

4 Software overhead in messaging layers: where does the time go?
Vijay Karamcheti, Andrew A. Chien
November 1994 **Proceedings of the sixth international conference on Architectural support for programming languages and operating systems**, Volume 29 , 28 Issue 11 , 5
Full text available: pdf(1.13 MB) Additional information: full citation, abstract, references, citings, index terms

Despite improvements in network interfaces and software messaging layers, software communication overhead still dominates the hardware routing cost in most systems. In this study, we identify the sources of this overhead by analyzing software costs of typical communication protocols built atop the active messages layer on the CM-5. We show that up to 50–70% of the software messaging costs are a direct consequence of the gap between specific network features such as arbitrary delivery ...

5 Hardware/Software Co-testing of Embedded Memories in Complex SOCs
Bai Hong Fang, Qiang Xu, Nicola Nicolici
November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided**

design
Full text available: pdf(145.78 KB) Additional information: full citation, abstract, index terms

A novel approach for testing embedded memories in complexsystems-on-a-chip (SOCs) is presented. The proposedsolution aims to balance the usage of the existing on-chipresources and dedicated design for test (DFT) hardwaresuch that the functional power constraints are not exceeddduring test while trading-off the testing time againstDFT area and performance overhead. The suitability ofsoftware-centric and hardware-centric approaches for embeddedmemory testing is examined and to combine the advanta ...

6 Issues in partitioning & design space eploration for codesign: Dynamic hardware/software partitioning: a first approach
Greg Stitt, Roman Lysecky, Frank Vahid
June 2003 **Proceedings of the 40th conference on Design automation**
Full text available: pdf(216.05 KB) Additional information: full citation, abstract, references, citings, index terms

Partitioning an application among software running on a microprocessor and hardware co-processors in on-chip configurable logic has been shown to improve performance and energy consumption in embedded systems. Meanwhile, dynamic software optimization methods have shown the usefulness and feasibility of runtime program optimization, but those optimizations do not achieve as much as partitioning. We introduce a first approach to dynamic hardware/software partitioning. We describe our system archit ...

Keywords: FPGA, codesign, dynamic optimization, embedded systems, hardware/software partitioning, platforms, self-improving chips, synthesis, system-on-a-chip

7 Implementing multidestination worms in switch-based parallel systems: architectural alternatives and their impact
Craig B. Stunkel, Rajeev Sivaram, Dhabaleswar K. Panda
May 1997 **ACM SIGARCH Computer Architecture News , Proceedings of the 24th annual international symposium on Computer architecture**, Volume 25 Issue 2
Full text available: pdf(1.84 MB) Additional information: full citation, abstract, references, citings, index terms

Multidestination message passing has been proposed as an attractive mechanism for efficiently implementing multicast and other collective operations on direct networks. However, applying this mechanism to switch-based parallel systems is non-trivial. In this paper we propose alternative switch architectures with differing buffer organizations to implement multidestination worms on switch-based parallel systems. First, we discuss issues related to such implementation (deadlock-freedom, replicatio ...

8 Hardware support for automatic routing
E. Damm, H. Gethöffer, K. Kaiser, E. Damm GmbH
January 1982 **Proceedings of the 19th conference on Design automation**
Full text available: pdf(210.55 KB) Additional information: full citation, abstract, references, citings, index terms

A system for automatic routing based on an iterative application of Lee's algorithm is presented. An extended cell admissibility is defined for continuous design rules in coarse rectangular grids. Combined hardware and software design strategies are applied towards the definition of data structures and their kernel primitives for automatic routing. The hardware architecture and the implementation of specific structures are discussed. The resulting extended routing unit is used in a CAD syst ...

9 CAD for reconfigurable computing: Dynamic FPGA routing for just-in-time FPGA compilation
Roman Lysecky, Frank Vahid, Sheldon X.-D. Tan
June 2004 **Proceedings of the 41st annual conference on Design automation - Volume 00**
Full text available: pdf(73.03 KB) Additional information: full citation, abstract, references, index terms

Just-in-time (JIT) compilation has previously been used in many applications to enable standard software binaries to execute on different underlying processor architectures. However, embedded systems increasingly incorporate Field Programmable Gate Arrays (FPGAs), for which the concept of a standard hardware binary did not previously exist, requiring designers to implement a hardware circuit for a single specific FPGA. We introduce the concept of a standard hardware binary, using a just-in-time ...

Keywords: FPGA, codesign, configurable logic, dynamic optimization, hardware/software partitioning, just-in-time compilation, place and route, platforms, system-on-a-chip, warp processors

10 A benchmark suite for evaluating configurable computing systems—status, reflections, and future directions
S. Kumar, L. Pires, S. Ponnuswamy, C. Nanavati, J. Golusky, M. Vojta, S. Wadi, D. Pandalai, H. Spaanenberg

February 2000 **Proceedings of the 2000 ACM/SIGDA eighth international symposium on Field programmable gate arrays**

This paper presents a benchmark suite for evaluating a configurable computing system's infrastructure, both tools and architecture. A novel aspect of this work is the use of stressmarks, benchmarks that focus on a specific characteristic or property of interest. This is in contrast to traditional approaches that utilize functional benchmarks, benchmarks that emphasize measuring end-to-end execution time. This suite can be used to assess a broad range of con ...

Keywords: adaptive computing ssytems, benchmarks, configurable computing systems, methodology, specifications, stressmarks

11 A secure distributed capability based system (extended abstract)
Howard L. Johnson, John F. Koegel, Rhonda M. Koegel
October 1985 **Proceedings of the 1985 ACM annual conference on The range of computing : mid-80's perspective: mid-80's perspective**

Keywords: capability architecture, computer security, distributed system security, network encryption

12 IP switching—ATM under IP
Peter Newman, Greg Minshall, Thomas L. Lyon
April 1998 **IEEE/ACM Transactions on Networking (TON)**, Volume 6 Issue 2

Keywords: Internet protocol, asynchronous transfer mode, broadband communication, communication system control, data communication, packet switching, protocols

13 Fast Evaluation of Protocol Processor Architectures for IPv6 Routing
Johan Lilius, Dragos Truscan, Seppo Virtanen
March 2003 **Proceedings of the conference on Design, Automation and Test in Europe: Designers' Forum - Volume 2**

In this paper we present a design case study in configuring our protocol processor architecture to meet the performance requirements of IPv6 routing at gigabit speeds. Our methodology makes it possible to make fast reliable analyses of the problem on a high level and to find its key bottlenecks and design constraints. Based on the analyses we suggest architectural configurations for the target application. The best configurations can then be further analyzed in more detailed system-level simulat ...

14 Wormhole IP over (connectionless) ATM
Manolis G. H. Katevenis, Iakovos Mavroidis, Georgios Sapountzis, Eva Kalyvianaki, Ioannis Mavroidis, Georgios Glykopoulos
October 2001 **IEEE/ACM Transactions on Networking (TON)**, Volume 9 Issue 5

High-speed switches and routers internally operate using fixed-size cells or segments; variable-size packets are segmented and later reassembled. Connectionless ATM was proposed to quickly carry IP packets segmented into cells (AAL5) using a number of hardware-managed ATM VCs. We show that this is analogous to wormhole routing. We modify this architecture to make it applicable to existing ATM equipment: we propose a low-cost, single-input, single-output Wormhole IP Router that functions as a VP/ ...

Keywords: Connectionless ATM, IP over ATM, gigabit router, routing filter, wormhole IP, wormhole routing

15 Scalable Hardware-Based Multicast Trees
Salvador Coll, Duato Duato, Fabrizio Petrini, Francisco J. Mora
November 2003 **Proceedings of the 2003 ACM/IEEE conference on Supercomputing**

This paper presents an algorithm for implementing optimal hardware-based multicast trees, on

networks that provide hardware support for collective communication. Although the proposed methodology can be generalized to a wide class of networks, we apply our methodology to the Quadrics network, a state-of-the-art network that provides hardware-based multicast communication. The proposed mechanism is intended to improve the performance of the collective communication patterns on the network, in tho ...

16 The transport layer: tutorial and survey
Sami Iren, Paul D. Amer, Phillip T. Conrad
December 1999 **ACM Computing Surveys (CSUR)**, Volume 31 Issue 4

Transport layer protocols provide for end-to-end communication between two or more hosts. This paper presents a tutorial on transport layer concepts and terminology, and a survey of transport layer services and protocols. The transport layer protocol TCP is used as a reference point, and compared and contrasted with nineteen other protocols designed over the past two decades. The service and protocol features of twelve of the most important protocols are summarized in both text and tables.< ...

Keywords: TCP/IP networks, congestion control, flow control, transport protocol, transport service

17 Scheduling computations on a software-based router
Xiaohu Qie, Andy Bavier, Larry Peterson, Scott Karlin
June 2001 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 2001 ACM SIGMETRICS international conference on Measurement and modeling of computer systems**, Volume 29 Issue 1

Recent efforts to add new services to the Internet have increased the interest in software-based routers that are easy to extend and evolve. This paper describes our experiences implementing a software-based router, with a particular focus on the main difficulty we encountered: how to schedule the router's CPU cycles. The scheduling decision is complicated by the desire to differentiate the level of service for different packet flows, which leads to two fundamental conflicts: (1) assigning proce ...

18 Case studies: A codesigned on-chip logic minimizer
Roman Lysecky, Frank Vahid
October 2003 **Proceedings of the 1st IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis**

Boolean logic minimization is traditionally used in logic synthesis tools running on powerful desktop computers. However, logic minimization has recently been proposed for dynamic use in embedded systems, including network route table reduction, network access control list table reduction, and dynamic hardware/software partitioning. These new uses require logic minimization to run dynamically as part of an embedded system's active operation. Performing such dynamic logic minimization on-chip gre ...

Keywords: dynamic optimization, embedded CAD, embedded systems, hardware/software codesign, logic minimization, on-chip logic minimization, on-chip synthesis, system-on-a-chip

19 CRUSADE: hardware/software co-synthesis of dynamically reconfigurable heterogeneous real-time distributed embedded systems
Bharat P. Dave
January 1999 **Proceedings of the conference on Design, automation and test in Europe**

20 Session 23: internal interconnect: Optimal software multicast in wormhole-routed multistage networks
Hong Xu, Ya-Dong Gui, Lionel M. Ni
November 1994 **Proceedings of the 1994 ACM/IEEE conference on Supercomputing**

Multistage interconnection networks are a popular class of interconnection architecture for constructing scalable parallel computers (SPCs). The focus of this paper is on wormhole routed multistage networks supporting turnaround routing. Existing machines characterized by such a system model include the IBM SP-1, TMC CM-5, and Meiko CS-2.Efficient collective communication among processor nodes is critical to the performance of SPCs. A system-level multicast service, in which the same message is ...

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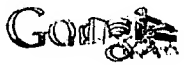

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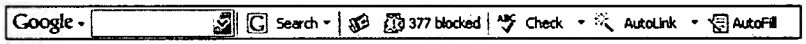

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1 Promises and reality: Server I/O networks past, present, and future
Renato John Recio
August 2003 **Proceedings of the ACM SIGCOMM workshop on Network-I/O convergence: experience, lessons, implications**
Full text available: pdf(225.62 KB) Additional Information: full citation, abstract, references, index terms

Enterprise and technical customers place a diverse set of requirements on server I/O networks. In the past, no single network type has been able to satisfy all of these requirements. As a result several fabric types evolved and several interconnects emerged to satisfy a subset of the requirements. Recently several technologies have emerged that enable a single interconnect to be used as more than one fabric type. This paper will describe the requirements customers place on server I/O networks; t ...

Keywords: 10 GigE, Cluster, Cluster Networks, Gigabit Ethernet, I/O Expansion Network, IOEN, InfiniBand, LAN, PCI, PCI Express, RDMA, RNIC, SAN, Socket Extensions, TOE, IONIC, iSCSI, iSER

2 Functional-join processing
R. Braumandl, J. Claussen, A. Kemper, D. Kossmann
February 2000 **The VLDB Journal — The International Journal on Very Large Data Bases**, Volume 8 Issue 3-4
Full text available: pdf(486.22 KB) Additional Information: full citation, abstract, citings, index terms

Inter-object references are one of the key concepts of object-relational and object-oriented database systems. In this work, we investigate alternative techniques to implement inter-object references and make the best use of them in query processing, i.e., in evaluating functional joins. We will give a comprehensive overview and performance evaluation of all known techniques for simple (single-valued) as well as multi-valued functional joins. Furthermore, we will describe special *order-preser ...*

Keywords: *Functional join, Logical OID, Object identifier, Order-preserving join, Physical OID, Pointer join, Query processing*

3 Reducing Address Bus Transitions for Low Power Memory Mapping
Preeti R. Panda, Nikil D. Dutt
March 1996 **Proceedings of the 1996 European conference on Design and Test**

Full text available: pdf(713.02 KB) Additional Information: full citation, abstract, citings
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We present low power techniques for mapping arrays in behavioral specifications to physical memory, specifically for memory intensive behaviors that exhibit regularity in their memory access patterns. Our approach exploits this regularity in memory accesses by reducing the number of transitions on the memory address bus. We study the impact of different strategies for mapping arrays in behaviors to physical memory, on power dissipation during memory accesses. We describe a heuristic for selectin ...

4 A simple and efficient parallel disk mergesort
Rakesh D. Barve, Jeffrey Scott Vitter
June 1999 **Proceedings of the eleventh annual ACM symposium on Parallel algorithms and architectures**
Full text available: pdf(1.32 MB) Additional Information: full citation, references, citings, index terms

5 Shared virtual memory with automatic update support
Liviu Iftode, Matthias Blumrich, Cezary Dubnicki, David L. Oppenheimer, Jaswinder Pal Singh, Kai Li
May 1999 **Proceedings of the 13th international conference on Supercomputing**
Full text available: pdf(1.20 MB) Additional Information: full citation, references, index terms

6 A comparative study of arbitration algorithms for the Alpha 21364 pipelined router
Shubhendu S. Mukherjee, Federico Silla, Peter Bannon, Joel Emer, Steve Lang, David Webb
October 2002 **Proceedings of the 10th international conference on Architectural support for programming languages and operating systems**, Volume 30 , 36 , 37 Issue 5 , 5 , 10
Full text available: pdf(1.44 MB) Additional Information: full citation, abstract, references

Interconnection networks usually consist of a fabric of interconnected routers, which receive packets arriving at their input ports and forward them to appropriate output ports. Unfortunately, network packets moving through these routers are often delayed due to conflicting demand for resources, such as output ports or buffer space. Hence, routers typically employ *arbiters* that resolve conflicting resource demands to maximize the number of matches between packets waiting at input ports an ...

7 Exploiting the locality of memory references to reduce the address bus energy
Enric Musoll, Tomás Lang, Lordi Cortadella
August 1997 **Proceedings of the 1997 international symposium on Low power electronics and design**
Full text available: pdf(933.21 KB) Additional Information: full citation, references, citings

8 A personal supercomputer for climate research
James C. Hoe, Chris Hill, Alistair Adcroft
January 1999 **Proceedings of the 1999 ACM/IEEE conference on Supercomputing (CDROM)**
Full text available: pdf(491.63 KB) Additional Information: full citation, references, index terms

9

Detecting graph-based spatial outliers: algorithms and applications (a summary of results)
Shashi Shekhar, Chang-Tien Lu, Pusheng Zhang
August 2001 **Proceedings of the seventh ACM SIGKDD international conference on Knowledge discovery and data mining**
Full text available: pdf(590.38 KB) Additional Information: full citation, abstract, references, citings, index terms

Identification of outliers can lead to the discovery of unexpected, interesting, and useful knowledge. Existing methods are designed for detecting spatial outliers in multidimensional geometric data sets, where a distance metric is available. In this paper, we focus on detecting spatial outliers in graph structured data sets. We define statistical tests, analyze the statistical foundation underlying our approach, design several fast algorithms to detect spatial outliers, and provide a cost model ...

Keywords: Outlier Detection, Spatial Data Mining, Spatial Graphs

10 Special system-oriented section: the best of SIGMOD '94: QuickStore: a high performance mapped object store
Seth J. White, David J. DeWitt
October 1995 **The VLDB Journal — The International Journal on Very Large Data Bases**, Volume 4 Issue 4
Full text available: pdf(2.58 MB) Additional Information: full citation, abstract, references, citings

QuickStore is a memory-mapped storage system for persistent C++, built on top of the EXODUS Storage Manager. QuickStore provides fast access to in-memory objects by allowing application programs to access objects via normal virtual memory pointers. This article presents the results of a detailed performance study using the OO7 benchmark. The study compares the performance of QuickStore with the latest implementation of the E programming language. The QuickStore and E systems exemplify the two ba ...

Keywords: benchmark, client-server, memory-mapped, object-oriented, performance, pointer swizzling

11 Set-associative cache simulation using generalized binomial trees
Rabin A. Sugumar, Santosh G. Abraham
February 1995 **ACM Transactions on Computer Systems (TOCS)**, Volume 13 Issue 1
Full text available: pdf(1.51 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Set-associative caches are widely used in CPU memory hierarchies, I/O subsystems, and file systems to reduce average access times. This article proposes an efficient simulation technique for simulating a group of set-associative caches in a single pass through the address trace, where all caches have the same line size but varying associativities and varying number of sets. The article also introduces a generalization of the ordinary binomial tree and presents a representation of caches in ...

Keywords: all-associativity simulation, binomial tree, cache modeling, inclusion properties, set-associative caches, single-pass simulation, trace-driven simulation

12 IO-Lite: a unified I/O buffering and caching system
Vivek S. Pai, Peter Druschel, Willy Zwaenepoel
February 2000 **ACM Transactions on Computer Systems (TOCS)**, Volume 18 Issue 1

Full text available: pdf(196.15 KB) Additional Information: full citation, abstract, references, citings, index terms

This article presents the design, implementation, and evaluation of IO -Lite, a unified I/O buffering and caching system for general-purpose operating systems. IO-Lite unifies all buffering and caching in the system, to the extent permitted by the hardware. In particular, it allows applications, the interprocess communication system, the file system, the file cache, and the network subsystem to safely and concurrently share a single physical copy of the data. Protection and ...

Keywords: I/O buffering, caching, networking, zero-copy

13 Session 7: Reducing transitions on memory buses using sector-based encoding technique
Yazdan Aghaghiri, Massoud Pedram, Farzan Fallah
August 2002 **Proceedings of the 2002 international symposium on Low power electronics and design**
Full text available: pdf(266.67 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we introduce a class of irredundant low power encoding techniques for memory address buses. The basic idea is to partition the memory space into a number of sectors. These sectors can, for example, represent address spaces for the code, heap, and stack segments of one or more application programs. Each address is first dynamically mapped to the appropriate sector and then is encoded with respect to the sector head. Each sector head is updated based on the last accessed address in ...

14 Equal rights for functional objects or, the more things change, the more they are the same
Henry G. Baker
October 1993 **ACM SIGPLAN OOPS Messenger**, Volume 4 Issue 4
Full text available: pdf(2.61 MB) Additional Information: full citation, abstract, index terms

We argue that intensional *object identity* in object-oriented programming languages and databases is best defined operationally by side-effect semantics. A corollary is that "functional" objects have extensional semantics. This model of object identity, which is analogous to the normal forms of relational algebra, provides cleaner semantics for the value-transmission operations and built-in primitive equality predicate of a programming language, and eliminates the confusion surrounding "ca ...

15 Compiler-based I/O prefetching for out-of-core applications
Angela Demke Brown, Todd C. Mowry, Orran Krieger
May 2001 **ACM Transactions on Computer Systems (TOCS)**, Volume 19 Issue 2
Full text available: pdf(499.03 KB) Additional Information: full citation, abstract, references, citings, index terms, review

Current operating systems offer poor performance when a numeric application's working set does not fit in main memory. As a result, programmers who wish to solve "out-of-core" problems efficiently are typically faced with the onerous task of rewriting an application to use explicit I/O operations (e.g., read/write). In this paper, we propose and evaluate a fully automatic technique which liberates the programmer from this task, provides high performance, and requires only minima ...

Keywords: compiler optimization, prefetching, virtual memory

16 Emulation - a useful tool in the development of computer systems

F. A. Salomon, D. A. Tafuri
March 1982 **Proceedings of the 15th annual symposium on Simulation**

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Emulation is playing a key role in the development of a BELLMAC-32A microprocessor-based computer system at Bell Telephone Laboratories. The emulation is used for the development of the operating system for the new computer system to permit both hardware and software development to proceed in parallel. The emulation's goal is to permit the operating system to be developed before the hardware is available. This is aimed at reducing the time and effort required in the hardware/software integr ...

17 Fast cluster failover using virtual memory-mapped communication
Yuanyuan Zhou, Peter M. Chen, Kai Li
May 1999 **Proceedings of the 13th international conference on Supercomputing**

Full text available: pdf(1.45 MB) Additional Information: full citation, references, citings, index terms

18 Cache memory performance in a unix enviroment
Cedell Alexander, William Keshlear, Furrokh Cooper, Faye Briggs
June 1986 **ACM SIGARCH Computer Architecture News**, Volume 14 Issue 3

Full text available: pdf(2.10 MB) Additional Information: full citation, citings, index terms

19 High-level low power design II: A VLSI array processing oriented fast fourier transform algorithm and hardware implementation
Zhenyu Liu, Yang Song, Takeshi Ikenaga, Satoshi Goto
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Many parallel Fast Fourier Transform (FFT) algorithms adopt multiple stages architecture to increase performance. However, data permutation between stages consumes volume memory and processing time. An FFT array processing mapping algorithm is proposed in this paper to overcome this demerit. In this algorithm, arbitrary 2^k butterfly units (BUs) could be scheduled to work in parallel on $n=2^s$ data ($k=0, 1,..., s-1$). Because no inter stage data transfer is required, mem ...

Keywords: array processing, fast fourier transform (FFT), singleton algorithm

20 Coherent network interfaces for fine-grain communication
Shubhendu S. Mukherjee, Babak Falsafi, Mark D. Hill, David A. Wood
May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd annual international symposium on Computer architecture**, Volume 24 Issue 2

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Historically, processor accesses to memory-mapped device registers have been marked uncachable to insure their visibility to the device. The ubiquity of snooping cache coherence, however, makes it possible for processors and devices to interact with cachable, coherent memory operations. Using coherence can improve performance by facilitating burst transfers of whole cache blocks and reducing control overheads (e.g., for polling).This paper begins an exploration of network interfaces (NIs) that u ...

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